PATENT ATTORNEY DOCKET NO.: N1085-00192
[TSMC2003-0289]

III. Remarks

Applicants are grateful to the Examiner for allowing Claims 1-28 and 32. Reconsideration and withdrawal of the rejection of Claims 29-31 and 33-34 are respectfully requested in view of the following arguments.

A. Rejection under 35 U.S.C. § 112

The Action rejects Claim 30 as being indefinite under §112, ¶2. The Examiner indicates that the phrase "any undercut" is indefinite because Claim 29 recites "without undercut."

Claim 29 recites the isolation layer being "**substantially** without undercut." Applicants submit that the phrase "substantially without undercut" permits no undercut, or some undercut. Indeed, the Federal Circuit recently recognized that, for example, "substantially flattened surface" covered both perfectly flattened surfaces and surfaces with some degree of curvature. See Playtex Prods., Inc. v. Procter & Gamble Co., 2005 U.S. App. Lexis 3693, *22-23 (Fed Cir. March 7, 2005). Claim 30 further recites that "any undercut" (i.e., when the isolation layer of Claim 29 has some undercut, but is "substantially without undercut") of the isolation layer of Claim 29 has a lateral depth of less than 100Å. It is submitted, therefore, that the recitation "any undercut" is sufficiently definite under §112, ¶2. Reconsideration and withdrawal of this rejection are respectfully requested.

B. Rejection under 35 U.S.C. § 102

The Action rejects Claims 29, 31 and 33 as being anticipated by U.S. Patent No. 6,562,665 to Yu.

With respect to method Claim 33, Claim 33 recites step (d): "performing a cleaning process prior to forming said gate dielectric layer, wherein said sacrificial layer is formed to a thickness sufficient to substantially protect said at least one conductive region from undercut in the isolation layer from said cleaning process." Applicants submit that Yu does not expressly

disclose a "cleaning process" as would be understood by those in the art nor, it follows, does it teach a sacrificial layer that protects the isolation layer from undercut from a cleaning process.

In rejecting Claim 31, the Examiner cites to Column 6, Line 63 to Column 7, Line 3 of Yu. These sections describe the transition from FIG. 11 to FIG. 12 of Yu. Specifically, the first spacers 328, second spacers 334 and cap layer 310 are etched away to leave pillar 314 on the buried insulator layer 302. Yu provides no details for these etch process, indicating only that the processes "are known to one of ordinary skill in the art." (Column 7, Lines 2-3).

The etch processes described by Yu are primary etch processes for removing deposited layers, not cleaning processes. As Applicants point out in the description of the present application, cleaning processes are sometimes employed after removal of layers (such as cap dielectric layers) by etch processes to clean the substrate prior to subsequent deposition steps (e.g., depositing the gate dielectric layer). (See ¶¶3, 21). It is submitted that one of ordinary skill would not understand the primary etch processes of Yu, which removes spacers 328, spacers 334 and cap layer 310 to be "cleaning processes."

Indeed, in rejecting Claim 34, the Examiner cites to U.S. Patent No. 6,489,201 to Yoon for teaching a HF "cleaning process." In FIG. 1D, Yoon shows that a contact hole is etched to expose bit line plug 20. (Column 2, Lines 22-25). This etch process is readily seen by comparing FIGS. 1C and 1D. Yoon then states: "Referring to FIG. 1E, after performing a cleaning process using hydrofluoric acid (HF) for removing a native oxide film remaining on bit line plug 20, a barrier metal layer 30 . . . is deposited [followed by] a tungsten layer 32." (Column 2, Lines 26-31). Yoon clearly indicates that "cleaning processes" are not primary etch processes, but rather processes that clean debris and other undesired etch byproducts (such as native oxides) that remain after primary etching. Comparing FIGS. 1D to 1E shows that no layers shown in the figures are removed by the "cleaning process." Rather, FIG. 1D and FIG. 1E are identical, except for the post-cleaning deposition of layers 30 and 32 and the damage in region A caused by the cleaning process. (Column 2, Lines 57-59).

Therefore, Yu does not expressly describe a "cleaning process" when it describes the etching processes for removing first spacers 328, second spacers 334 and cap layer 310. If one of ordinary skill were to understand that cleaning processes typically occur after such etch process, and keeping in mind that Yu is silent as to any cleaning processes, it is submitted that Yu provides no teaching or suggestion to leave sufficient amounts of dielectric 328, 334 after etching to protect the isolation layer 302 of Yu from the cleaning process. Put another way, if Yu's methodology conforms to conventional processes, layers 328 and 334 would be removed, then a cleaning process would be employed (which would create an undercut in isolation layer 302), followed by formation of dielectric layer 342 (FIG. 14).

For at least these reasons, it is submitted that Claim 33 is not anticipated.

Claim 29 is directed to an integrated circuit where the isolation layer is substantially without undercut at the region within the isolation layer beneath the conductive region. As indicated in Applicants' background section, a cleaning process typically follows removal of a cap dielectric layer, such as layer 310 shown in FIG. 11 of Yu. As described above, Applicants submit that any such cleaning process would occur after the removal of first spacers 328, second spacers 334 and cap layer 310, thereby causing undercuts in isolation layer 302. For at least these reasons, it is submitted that Claim 29 is not anticipated by the cited reference.

Claim 31 depends from Claim 29 and is, therefore, also allowable. Still further, Claim 31 recites that the conductive region has a "mesa structure." Applicants submit that it has distinguished a non-mesa structure (rectangular element 120 of FIG. 1 having vertical sidewalls) from a mesa structure (trapezoidal element 225 of FIG. 2G). As explained in ¶15 of the present application, providing conductive regions with a mesa structure or shape provides advantages for subsequent processing, such as improved etch margin for pattering the gate and/or the enhanced filling ability of and interlayer dielectric (ILD) between active regions.

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Referring to FIG. 12 of Yu, active region 314 clearly has vertical walls. This generally rectangular shape is not a "mesa structure" as defined by Applicants. For at least these additional reasons, it is submitted that Claim 31 is allowable over the art of record.

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IV. Conclusion

In view of the foregoing remarks and amendments, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account **04-1679**.

Respectfully submitted,

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